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EXAMINER	
HIGA, BRENDAN Y	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/748,780	CHANDRA ET AL.	
	Examiner	Art Unit	
	BRENDAN HIGA	2453	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7-18,20-30,32-35,37-39 and 41-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7-18,20-30,32-35,37-39 and 41-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to Applicant's amendment and request for reconsideration filed on July 08, 2010.

Claims 1, 10, 11, 18, 23, 30, 35, 42 and 44 have been amended.

Claims 2, 6, 19, 31, 36 and 40 have been canceled.

Claims 1, 3-5, 7-18, 20-30, 32-35, 37-39, 41-48 are currently pending.

Claim Interpretation

As per claims, 1, 10, 18, 23, 30, 35, and 42 Applicant's amendments including *"wherein the at least a portion of received content is to be distributed across a plurality of non-contiguous locations within the at least one memory channel if the at least portion of received content exceeds the capacity of a single contiguous location within the at least one memory channel to meet the throughput and based, at least in part, on whether a packet meta data can be distributed in a way to meet the throughput"* simply states an intended use of "the at least a portion of received content" that is outside the scope of Applicant's claimed invention and has therefore not been given patentably weight consistent with MPEP § 2111.04.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1, 3-5 and 7-9 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1, 3-5 and 7-9 are directed to a method. However, in *In re Bilski*, 545 F.3d 943 (Fed. Cir. 2008) the Court set out the "machine-or-transformation test" (i.e., *"a claimed process is surely patent-eligible under §101 if: (1) it is tied to a particular machine or apparatus, or (2) it transforms a particular article into a different state or thing." Id.* at 956).

Here, the method performed by claim 1 is not tied to a particular machine - the claim is silent as to a machine that performs the "comparing" and "determining" steps. Thus the broadest reasonable interpretation of the claim could include mental steps for performing said "comparing" and "determining". Furthermore, claim 1 does not otherwise transform a particular article into a different state or thing. Thus, claim 1, fails the machine or transformation test set out by the Federal Circuit in *Bilski.*

Furthermore, though the Supreme Court later held in *In re Bilski*, 130 S.Ct. 3218 (2010) that "the machine-or-transformation" is not the sole test for patent eligibility under §101 *Id.* at 3223, the majority of the Court consistently holds that processes directed to mental steps *per se*, as is the case here, are never patent eligible (*Id.* at 3255 (STEVENS, J., GINSBURG, J., BREYER, J., and SOTOMAYER, J., concurring) *"phenomena of nature …, mental processes, and abstract intellectual concepts are not patentable"*; and *Id.* at 3258 (BREYER, J., and SCALIA, J. concurring) *"In particular, the*

Court has long held that phenomena of nature, though just discovered, mental processes, and abstract intellectual concepts are not patentable under §101").

Dependent claim(s) 3-5 and 7-9 when analyzed as a whole are held to be patent ineligible under 35 U.S.C. 101 because the additional recited limitation(s) fail(s) to establish that the claim(s) are not directed to steps involved in a mental process.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 18, 20, 21, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Kadambi et al. (US 6,707,817)("Kadambi").

As per claim 18, Kadambi teaches an apparatus comprising:

A memory, including at least one memory channel (i.e. a Central Buffer Pool see Fig. 1, ref. 50); and

A routing manager (see Central Buffer Manager, col. 16, lines 45-48), communicatively coupled with the memory, to distribute at least a portion of received content to the at least one memory channel (see abstract *"determining whether the*

network switch has sufficient memory capacity to process the data packet", also see col. 16, lines 41-48) to meet a throughput (see col. 1, lines 18-25, gigabit ethernet environments).

As per claim 20, Kadambi further teaches:

a memory to store content, at least a subset if which is executable content (i.e. [executable] rules for controlling packet processing, see col. 5, lines 8-10); and

a control logic communicatively, coupled with the memory, to selectively execute at least a subset of the executable content, to implement an instance of the routing manager (see col. 5, lines 8-10, wherein the CPU 52 can be used as necessary to program SOC 10 with rules which are appropriate to control packet processing, read as programming the SOC 10 with control logic to execute the functions of the CBM).

As per claim 21, Kadambi further teaches wherein the control logic is implemented in a network processor (see "switch-on-chip", see Fig. 1, and col. 4, line 61-col. 5, line 24).

As per claim 22, Kadambi further teaches wherein the memory is static random access memory (see SRAM col. 7, line 22).

Claims 23-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Sindhu et al. (US 5,905,725)("Sindhu").

As per claim 23, Sindhu teaches an apparatus comprising:

Memory, including at least one memory channel (see Fig. 2B, ref. 104); and

an access manager (output request processor 1706, see col. 11, lines 1-7), communicatively coupled with the memory, to read at least a portion of received content from the memory channel (see col. 2, lines 29-30, "retrieving the data packet from non-contiguous locations in memory"); and

combining the at least portion of received content as if the at least portion of received content were distributed to a single contiguous location within the at least one memory channel (see col. 11, line 63 - col. 12, line 6, wherein the non-contiguous cells are thereafter combined to generate a proper packet for transfer out of router 20 on the line output interface).

As per claim 24, Sindhu further teaches wherein the access manager presents the at least portion of received content to an agent (i.e. an output formatter see Fig. 19, 1714, also see col. 11, lines 63-65).

As per claim 25, Sinhu further teaches wherein the at least portion of received content is packet meta data (see col. 12, lines 7-25 "routing packets", read as packet meta data), which includes a packet handle, the packet handle 1:1 mapped to the packet meta data (see col. 12, lines 7-25 and col. 4, lines 31-38, wherein the packet meta data includes "key information" read as a packet handle).

As per claim 26, Sindhu further teaches wherein the access manager uses the packet handle to locate and read the packet meta data from the at least one memory channel (see col. 12, lines 26-35)

As per claim 27, Sindhu further teaches the apparatus further comprising:

a memory to store content, at least a subset of which is executable content (see col. 11, lines 1-7, wherein the output request processor implied requires memory and executable content to perform the intended output request functions); and a control logic, communicatively coupled with the memory, to selectively execute at least a subset of the executable content, to implement an instance of the access manager see col. 11, lines 1-7, wherein the output request processor implied requires executable control logic to perform the intended output request functions).

As per claim 28, Sindhu further teaches wherein the method is implemented in a network processor (see output processor Fig. 5A ref. 505).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3, 7, 8, 9, 30, 33, 34, 35, 37 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadambi et al. (US 6,707,817)("Kadambi") in further view of Chin et al. (US 2006/0221945) ("Chin").

As per claim 1, Kadambi teaches a method comprising:

comparing the size of at least a portion of received content to a capacity of at least one memory channel (see abstract *"determining whether the network switch has sufficient memory capacity to process the data packet"*) to meet a given throughput (see col. 1, lines 18-25, gigabit ethernet environments); and determining whether to distribute the at least portion of received content across the at least one memory channel based, at least in part, on the comparison (see col. 16, lines 45-48, "If sufficient memory is

available in CBP 50 (Common Buffer Pool) for storage and identification of the incoming data packet, CBM 71 (Central Buffer Manager) places the data cell information (i.e. the series of linked cells that make up the data packet) on CPS channel 80 (Cell Protocol Sideband Channel)").

As per claim 1, Kadambi does not expressly teach wherein the comparison is with regard to a single contiguous location within the memory channel.

Nevertheless in the same art of packet switching, Chin teaches a system within a network switch that provides a mechanism for determining when a contiguous bank of buffer (i.e. a memory channel) is available for receiving a data packet (i.e. at least a portion of received content) (see ¶0006-¶0007, also see Provisional Application 60/464462 page, "Summary of the invention" pages 2-3, which discloses the buffer as comprising contiguous memory as well as the mechanism (i.e. buffer usage count) for determining whether buffer space is free, also see page 15, lines 5-6, *"In such an embodiment, a buffer might be considered empty and available for re-use when the current count for that buffer falls to 0"*). In particular, Chin teaches that because sequential data units of a given incoming data packet are written into contiguous banks of each buffer in the shared memory 114, there is no need for sequential data units of the packet to include linking information, in the shared memory 114, indicating where to find each next sequential data unit (see ¶0038, also see Provisional Application 60/464462 page 10, lines 15-20).

Thus, a person having ordinary skill in the art would have been motivated to modify the teachings of Kadambi with the teachings of Chin for modifying the Kadambi's

CBM 71 for not only determining whether there is sufficient memory channel capacity for an incoming data packet, but also to determine whether there is sufficient contiguous memory for processing the received data packet. The motivation for doing so would have been to reduce the burden for storing linking information, which in some prior art system may occupy up to 20 percent of the space in the shared memory (see Chin ¶0038).

As per claim 3, Kadambi further teaches wherein the at least portion of received content is a packet meta data (i.e. "header information", see col. 14, lines 26-27)

As per claim 7, Kadambi further teaches wherein the given throughput is communication channel speed (see col. 1, lines 18-25, gigabit ethernet environments).

As per claim 8, Kadambi further teaches wherein the method is implemented in a network process (see "switch-on-chip", see Fig. 1, and col. 4, line 61-col. 5, line 24).

As per claim 9, Kadambi further teaches wherein the determining whether to distribute occurs at start-up (see col. 5, lines 8-10, wherein the CPU is configured with rules [at start-up] for performing the packet processing (i.e. for making the determination as to whether to distribute)).

As per claim 30, Kadambi teaches a system comprising:

a memory, including at least one memory channel ("Common Buffer Pool", see Fig. 1, ref. 50); and

a routing manager (see Central Buffer Manager, col. 16, lines 45-48) coupled with the memory to selectively distribute at least a portion of received content to the at least one memory channel (see abstract *"determining whether the network switch has sufficient memory capacity to process the data packet"*) to meet a given throughput (see col. 1, lines 18-25, gigabit ethernet environments).

However, Kadambi does not expressly teach, wherein distributing the at least portion of received content is based in part on whether the at least portion of received content exceeds a capacity of a single contiguous location within the at least one memory channel.

Nevertheless in the same art of packet switching, Chin teaches a system within a network switch that provides a mechanism for determining when a contiguous bank of buffer (i.e. a memory channel) is available for receiving a data packet (see ¶0006-¶0007 wherein impliedly if the mechanism indicates that a contiguous bank of buffer is not available (i.e. the portion of received content would exceed a single contiguous location within at least one memory channel) the data packet will not be distributed, *read as distributing received content based at least in part on whether the at least portion of received content exceeds a capacity of a single contiguous location within the at least one memory channel*). Furthermore, Chin teaches that because sequential data units of a given incoming data packet are written into contiguous banks of each buffer in the shared memory 114, there is no need for sequential data units of the packet to include

linking information, in the shared memory 114, indicating where to find each next sequential data unit (see ¶0038).

Thus, a person having ordinary skill in the art would have been motivated to modify the teachings of Kadambi with the teachings of Chin for modifying Kadambi's CBM 71 for not only determining whether there is sufficient memory channel capacity for an incoming data packet, but also to determine whether the data packet will exceed the size of contiguous memory within the available memory. The motivation for doing so would have been to reduce the burden for storing linking information, which in some prior art system may occupy up to 20 percent of the space in the shared memory (see Chin ¶0038).

As per claim 33, Kadambi further teaches wherein the routing manager is implemented in a network process (see "switch-on-chip", see Fig. 1, and col. 4, line 61-col. 5, line 24).

As per claim 34, Kadambi further teaches wherein the memory is static random access memory (see 'SRAM type memory', col. 7, line 43).

As per claim 35, Kadambi teaches a non-transitory storage medium comprising content, which, when executed by a machine, causes the machine to:

compare the size of at least a portion of received content to a capacity of at least one memory channel (see abstract *"determining whether the network switch has*

sufficient memory capacity to process the data packet") to meet a given throughput (see col. 1, lines 18-25, gigabit ethernet environments); and

determine whether to distribute the at least portion of received content across the at least one memory channel based, at least in part, on the comparison (see col. 16, lines 45-48, "If sufficient memory is available in CBP 50 (Common Buffer Pool) for storage and identification of the incoming data packet, CBM 71 (Central Buffer Manager) places the data cell information (i.e. the series of linked cells that make up the data packet) on CPS channel 80 (Cell Protocol Sideband Channel)").

As per claim 35, Kadambi does not expressly teach wherein the comparison is with regard to a single contiguous location within the memory channel.

Nevertheless in the same art of packet switching, Chin teaches a system within a network switch that provides a mechanism for determining when a contiguous bank of buffer (i.e. a memory channel) is available for receiving a data packet (i.e. at least a portion of received content) (see ¶0006-¶0007). In particular, Chin teaches that because sequential data units of a given incoming data packet are written into contiguous banks of each buffer in the shared memory 114, there is no need for sequential data units of the packet to include linking information, in the shared memory 114, indicating where to find each next sequential data unit (see ¶0038).

Thus, a person having ordinary skill in the art would have been motivated to modify the teachings of Kadambi with the teachings of Chin for modifying the Kadambi's CBM 71 for not only determining whether there is sufficient memory channel capacity for an incoming data packet, but also to determine whether there is sufficient contiguous

memory for processing the received data packet. The motivation for doing so would have been to reduce the burden for storing linking information, which in some prior art system may occupy up to 20 percent of the space in the shared memory (see Chin ¶0038).

As per claim 37, Kadambi further teaches wherein the at least portion of received content is a packet meta data (i.e. "header information", see col. 14, lines 26-27)

As per claim 41, Kadambi further teaches wherein the given throughput is communication channel speed (see col. 1, lines 18-25, gigabit ethernet environments).

Claims 4, 5, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadambi et al. (US 6,707,817)("Kadambi") in further view of Chin et al. (US 2006/0221945) ("Chin"), in view of Sindhu et al. (US 5,905,725)("Sindhu"), in further view of Mullendore et al. (US 7,227,841) ("Mullendore").

As per claims 4 and 38, the combination of Kadambi, Chin and Sindhu does not expressly wherein the capacity of the single contiguous location within the at least one memory channel to meet the given throughput is less than 32 bytes.

Nevertheless, in the same art of network routing, Hochschild teaches a packet switch having a central queue (i.e. at least one memory channel) capable of processing incoming packets in 8-byte chunks, thus requiring only 8-byte capacity of contiguous

memory for processing each chunk in the central queue (see col. 5, lines 40-col. 6, line 20, col. 12, lines 1-27, also see col. 23, lines 4-20).

A person having ordinary skill in the art would have been motivated to modify the teachings of Kadambi, Chin and Sindhu with the teachings of Hochschild for using contiguous block of memory less than 32 bytes to meet a given throughput. The motivation for doing so would have been to enable the system in Kodambi to processor packets of data that do not require a full 32 bytes of contiguous memory.

As per claims 5 and 39, Kadambi further teaches wherein the a memory size of the packet meta data is at least 32 bytes (see 64 bytes, col. 14, lines 26-27)

Claims 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadambi et al. (US 6,707,817)("Kadambi") in further view of Chin et al. (US 2006/0221945) ("Chin"), in further view of Mullendore et al. (US 7,227,841) ("Mullendore").

As per claim 32, the combination of Kadambi and Chin does not expressly wherein the capacity of the single contiguous location within the at least one memory channel to meet the given throughput is less than 32 bytes.

Nevertheless, in the same art of network routing, Hochschild teaches a packet switch having a central queue (i.e. at least one memory channel) capable of processing incoming packets in 8-byte chunks, thus requiring only 8-byte capacity of contiguous memory for processing each chunk in the central queue (see col. 5, lines 40-col. 6, line 20, col. 12, lines 1-27, also see col. 23, lines 4-20).

A person having ordinary skill in the art would have been motivated to modify the teachings of Kadambi, Chin and Sindhu with the teachings of Hochschild for using contiguous block of memory less than 32 bytes to meet a given throughput. The motivation for doing so would have been to enable the system in Kodambi to processor packets of data that do not require a full 32 bytes of contiguous memory.

Claims 10-17 and 42-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sindhu et al. (US 5,905,725)("Sindhu") in further view of Raad (US 2005/0050289)("Raad").

As per claim 10, Sindhu teaches a method comprising:

accessing at least a portion of received content distributed across at least at least on memory channel (see col. 2, lines 29-30, "retrieving the data packet from non-contiguous locations in memory"); and

combining the at least portion of received content as if the at least portion of received content were distributed to a single contiguous location within the at least one memory channel (see col. 11, line 63 - col. 12, line 6, wherein the non-contiguous cells are thereafter combined to generate a proper packet for transfer out of router 20 on the line output interface)

As per claim 10, Sindhu does not expressly teach wherein the at least portion of received content is read simultaneously across the at least one memory channel.

Nevertheless, in the same art of memory accessing, Raad teaches a system for improving memory bandwidth by configuring the system to read non-contiguous (i.e. odd or even) locations of the memory array (i.e. DDR memory) simultaneously (see ¶0005 and ¶0006).

A person having ordinary skill in the art would have been motivated to modify the teachings of Sindhu with the teachings of Raad for configuring Sindhu's system to simultaneously retrieve the data-packet portions from non-contiguous locations in memory. The motivation for doing so would have been to improve the overall memory bandwidth within Sindhu's system (see Raad ¶0005).

As per claim 11, Sindhu further teaches presenting the at least portion of received content to an agent (i.e. an output formatter see Fig. 19, 1714, also see col. 11, lines 63-65).

As per claim 12, Sinhu further teaches wherein the at least portion of received content is packet meta data (see col. 12, lines 7-25 "routing packets", read as packet meta data).

As per claim 13, Sindhu further teaches where the packet meta data includes a packet handle (see col. 12, lines 7-25, wherein the packet meta data includes "key information" read as a packet handle).

As per claim 14, Sindhu further teaches wherein the packet handle is 1:1 mapped to the packet meta data distributed across the at least one memory channel to facilitate the accessing of the packet meta data distributed across the at lest one memory channel (see col. 12, lines 26-35, wherein the packet handle (i.e. "key information", see col. 4, lines 31-39) is mapped 1:1 to the packet and facilitates the location and reading of the distributed packet).

As per claim 15, Sindhu further teaches wherein combining the packet meta data distributed across the at least one memory channel is accomplished by temporarily storing the recombined packet meta data in local memory (i.e. an output buffer 1712, see col. 11, lines 63-64).

As per claim 16, Sindhu further teaches wherein presenting the packet meta data is accomplished by making the recombined packet meta data, temporarily stored in local memory (i.e. an output buffer 1712, see col. 11, lines 63-64), available to an agent as if it were a cohesive self-contained unit (see col. 43-46, wherein the output formatter receives the cells in the same way it would has the packet been a cohesive self-contained unit).

As per claim 17, Sindhu further teaches wherein the method is implemented in a network processor (see output processor Fig. 5A ref. 505).

As per claim 42, Sindhu teaches a storage medium comprising content, which, when executed by a machine, causes the machine to:

access portions of received content distributed across at least one memory channel (see col. 2, lines 29-30, "retrieving the data packet from non-contiguous locations in memory"); and

combine the portions of received content, as if the portions of received content were distributed to a single contiguous location with the at least one memory channel (see col. 11, line 63 - col. 12, line 6, wherein the non-contiguous cells are thereafter combined to generate a proper packet for transfer out of router 20 on the line output interface).

As per claim 42, Sindhu does not expressly teach wherein the portions of received content are read simultaneously across the at least one memory channel.

Nevertheless, in the same art of memory accessing, Raad teaches a system for improving memory bandwidth by configuring the system to read non-contiguous (i.e. odd or even) locations of the memory array (i.e. DDR memory) simultaneously (see ¶0005 and ¶0006).

A person having ordinary skill in the art would have been motivated to modify the teachings of Sindhu with the teachings of Raad for configuring Sindhu's system to simultaneously retrieve the data-packet portions from non-contiguous locations in memory. The motivation for doing so would have been to improve the overall memory bandwidth within Sindhu's system (see Raad ¶0005).

As per claim 43, Sindhu further teaches presenting the at least portion of received content to an agent (i.e. an output formatter see Fig. 19, 1714, also see col. 11, lines 63-65).

As per claim 44, Sinhu further teaches wherein the at least portion of received content is packet meta data (see col. 12, lines 7-25 "routing packets", read as packet meta data).

As per claim 45, Sindhu further teaches where the packet meta data includes a packet handle (see col. 12, lines 7-25, wherein the packet meta data includes "key information" read as a packet handle).

As per claim 46, Sindhu further teaches wherein the packet handle is 1:1 mapped to the packet meta data distributed across the at least one memory channel to facilitate the accessing of the packet meta data distributed across the at lest one memory channel (see col. 12, lines 26-35, wherein the packet handle (i.e. "key information" see col. 4, lines 31-39) is mapped 1:1 to the packet and facilitates the location and reading of the distributed packet).

As per claim 47, Sindhu further teaches wherein combining the packet meta data distributed across the at least one memory channel is accomplished by temporarily

storing the recombined packet meta data in local memory (i.e. an output buffer 1712, see col. 11, lines 63-64).

As per claim 48, Sindhu further teaches wherein presenting the packet meta data is accomplished by making the recombined packet meta data, temporarily stored in local memory (i.e. an output buffer 1712, see col. 11, lines 63-64), available to an agent as if it were a cohesive self-contained unit (see col. 43-46, wherein the output formatter receives the cells in the same way it would has the packet been a cohesive self-contained unit).

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sindhu et al. (US 5,905,725)("Sindhu") in further view of Kokubo et al. (US 5,486,717) ("Kokubo").

As per claim 29 Sindhu does not expressly teach wherein the memory is static random access memory.

Nevertheless, static random access memory was well known in the art at the time of the invention. For example, Kokubo teaches the advantages of SRAM which provides a more stable storage state over other types of memory such as dynamic random access memory (see col. 1, lines 5-15).

A person having ordinary skill in the art would have been motivated to modify the teachings of Sindhu with the teachings of Kokubo by configuring the Sindhu's memory

104 as SRAM. The motivation for doing so would have been to provide a more stable storage state (see col. 1, lines 5-15).

Response to Arguments

Applicant's arguments filed July 08, 2010 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "*distributing across a plurality of non-contiguous locations within the at least one memory channel if the at least portion of received content exceeds the capacity of a single contiguous location within the at least one memory channel to meet the throughput and based, at least in part, on whether a packet meta data can be distributed in a way to meet the throughput*") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRENDAN HIGA whose telephone number is (571)272-5823. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Thomas can be reached on (571)272-6776. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOSEPH THOMAS/
Supervisory Patent Examiner, Art Unit 2453

/BRENDAN HIGA/
Examiner, Art Unit 2453